Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte ALAIN CARBILLET

_____

Appeal No.1998-3411
Application No.08/548,113

_____

ON BRIEF

_____

Before URYNOWICZ, KRASS, and FLEMING, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

Decision on Appeal

This appeal is from the final rejection of claims 8-17, all the claims pending in the application.

The invention pertains to an information processing system. Claim 8 is illustrative and reads as follows:

8. An information processing system comprising a plurality of modules and an inter-module bus, each respective one of the modules including a respective processor and a respective local bus, the respective local bus serving one or more respective peripherals, the inter-module bus serving as a temporary link between at least two of the modules, the inter-module bus being connected to each respective one of the modules via at least a respective two-way buffer stage, the system including circuitry for enabling the processor of any of the modules to become temporarily a master of the local bus of any other of the modules, so as to have direct access to the peripherals of the other of the modules, and for disconnecting the processor of the other module

from the local bus of the other module.

The references relied upon by the examiner are:

| | | |
|---|---|---|
| Bederman | 4,209,839 | Jun. 24 1980 |
| Persaud et al. (Persaud) | 4,368,514 | Jan. 11, 1983 |
| Hughes et al. (Hughes) | 4,481,578 | Nov. 6, 1984 |

Claims 8-11 and 14-17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Persaud in view of Bederman.

Claims 12 and 13 stand rejected under 35 U.S.C. 103 as being unpatentable over Persaud in view of Bederman and Hughes.

The respective positions of the examiner and the appellant with regard to the propriety of these rejections are set forth in the final rejection (Paper No. 12) and the examiner's answer (Paper No. 17) and the appellant's brief (Paper No. 16).

## The Involved Subject Matter

Appellant's invention and the disclosures of Bederman and Persaud are adequately summarized at pages 2 and 3 of the brief. Based on the nature of our opinion below, it is unnecessary to set forth a description of the invention of Hughes.

## Opinion

Appellant's only argument with respect to claims 8-11 and 14-17 is in the brief at page 4. It consists of the position that neither Persaud nor Bederman teaches or suggests the claimed subject matter comprising "any of the modules to become temporarily the master of the local bus of the other module so as

to have direct access to the peripherals of the other module". It is asserted that the expression "the processor of any of the modules to become temporarily the master etc." means that each of a plurality of modules has a respective processor that is capable of having direct access to the peripherals of another one of the modules. Appellant contends that both references teach systems having one single processor capable of accessing the memory of other processors and, consequently, that neither reference teaches nor suggests that any of the modules are capable of accessing another processor's memory.

We find this argument persuasive and are of the opinion that the rejection should not be sustained.

In the sentence bridging pages 3 and 4 of the answer, the examiner acknowledges that "Persaud does not teach any of the processor modules can access any of the other processor modules local bus."

With respect to Bederman, we agree with the examiner's position at page 7 of the answer that this reference teaches a means for sharing a first memory means in alternation between processors. As noted by the examiner, such language appears in Bederman in claim 1, specifically at lines 6 and 7. This language of claim 1 is supported by Figure 1 of Bederman because memory 4 can be shared by master processor 1 and slave processor 6, and memory 3 can be shared by master processor 1 and processor 5.

However, the above language in claim 1 of Bederman is not a teaching that either processor 5 or 6 can become temporarily a master processor such that processor 5 can access either memory 2 or 4 in addition to its own memory 3 or that processor 6 can access either memory 2 or 3 in addition to its own memory 4. To the contrary, in his ABSTRACT Bederman specifically teaches that two of the three processing units can access its own memory but not any other memory.

Whereas claims 12 and 13 dependent from claim 11, and we will not sustain the rejection of claim 11 over Persaud and Bederman as stated above, we will not sustain the rejection of claims 12 and 13 under 35 U.S.C. § 103 as obvious over Persaud, Bederman and Hughes.

REVERSED

| | | |
|---|---|---|
| STANLEY M. URYNOWICZ JR.<br>Administrative Patent Judge | ) | |
| ERROL A. KRASS<br>Administrative Patent Judge | ) | BOARD OF PATENT APPEAL AND INTERFERENCES |
| MICHAEL R. FLEMING<br>Administrative Patent Judge | ) | |

SU/RWK

CORPORATE PATENT COUNSEL
U S PHILIPS CORPORATION
580 WHITE PLAINS ROAD
TARRYTOWN NY 10591